REMARKS

The Specification

The Examiner has requested that the Application numbers of all three co-pending patent applications be cited in paragraphs [0015] and [0017]. In accordance with the Examiner's request, paragraphs [0015] and [0017] have been amended to include the co-pending Application numbers. The specification has been also amended to change FIG. 1 (paragraphs [0012] and [0013]) and Figure 1 (paragraph [0016]) into FIGS. 1a-1b. Accordingly, withdrawal of the objection is respectfully requested.

The Claims

Claims 1-18 are currently pending. Claims 14, 15, and 17 have been amended. Support for the change in claim 17 can be found in FIG. 1a, for example. Applicants respectfully request reconsideration of the application in response to the non-final Office Action.

Claim Objections

Claims 14 and 15 have been objected to due to the informalities. In accordance with the Examiner's suggestion, claims 14 and 15 have been amended to replace "method" with "system." Accordingly, withdrawal of the objection is respectfully requested.

Claim Rejections – 35 USC §102

Claims 1, 8, 10, 11, 16, and 17 have been rejected under 35 USC §102(e) as being anticipated by US Patent No. 6,990,646 B2 to Yoshikawa.

In rejecting claims 1 and 8, the Office has stated that "Yoshikawa discloses a method (claim 1) and a system (claim 8 – see also col. 3, ll. 45-50, which cites a program used in a system) of determining an optimized parameters (setup and hold time) for a circuit simulation...(c) calculating a current primary criteria (i.e., timing constraint) parameter from the circuit simulation with the initial minimum optimization parameters...simulating the circuit until the primary criteria parameter converges to a prescribed value...." Applicants respectfully disagree.

The Yoshikawa patent discloses a method and program for correcting setup time and hold time errors. In Yoshikawa's method, the hold time errors which exist under a plurality of timing constraints may be corrected by inserting one or more delay buffers in hold time error paths. The plurality of timing constraints, which appear to be viewed by the Office to correspond to the primary criteria parameter (PCP) of the presently claimed invention, are respectively determined at a plurality of operating modes (col. 2, l. 31-44). Then, the setup time and hold time errors are calculated for each of the timing constraints. As such, the timing constrains represent conditions required to calculate the setup time and hold time errors. In marked contrast, the presently claimed invention discloses methods and system that determine optimization parameters (OP), such as hold time and setup time, for a circuit simulation by iteration. At each iteration step, the current optimization parameters are calculated. Then, the PCP, which is the bisection error, is calculated under the current optimization parameters and it is checked if the PCP has converged into a prescribed value. As such, in sharp contrast to Yoshikawa's method, the PCP is calculated when the operation parameters are given. Accordingly, the Yoshikawa patent fails to teach the steps of "calculating a current primary criteria parameters from the circuit simulation with the initial minimum optimization parameters...simulating the circuit until the primary criteria parameter converges to a prescribed value" as recited in claim 1, and a computer program configured to execute the procedure "calculate a current primary criteria parameter from the circuit simulation with the initial minimum optimization parameter...simulate the circuit until the primary criteria parameter converges to a prescribed value" as recited in claim 8. As the cited reference fails to teach all of the features of the claimed invention, Applicants respectfully submit that claims 1 and 8 are not anticipated by the Yoshikawa patent, and claims 1 and 8 are patentable. Claims 10 and 11 depend from claim 8, rendering them also patentable for at least the same reasons.

In rejecting claim 16, the Office has stated that "Yoshikawa discloses a method of simultaneously determining an optimized parameter... (c) determining an ideal optimization parameter from the circuit simulation by further simulating the

circuit until a criterion parameter converges to a prescribed value...." Applicants respectfully disagree.

As set forth above, the Yoshikawa patent fails to teach the step of "determining an ideal optimization parameter from the circuit simulation by further simulating the circuit until a criterion parameter converges to a prescribed value" as recited in claim 16. As such, Applicants respectfully submit that claim 16 is not anticipated by the Yoshikawa patent, and claim 16 is patentable. Claim 17 depends from claim 16, rendering it also patentable for at least the same reasons.

Claim 17 has been rejected by the same reasons as applied to reject claim 1. As claim 1 is not anticipated by the Yoshikawa patent, Applicants respectfully submit that claim 17 is not anticipated by the Yoshikawa patent, and claim 17 is allowable.

Claims 2-7, 9, 12-15, and 18 have been rejected under 35 U.S.C. §103(a) as being obvious over Yoshikawa in view of U.S. Patent No. 6,249,901 to Yuan et al. Applicants respectfully traverse this rejection.

The present application is assigned to Legend Design Technology Inc., as evidence by the Assignment recorded at Reel 014783/Frame 0082. The present application and the Yuan et al. patent were, at the time the invention of the present application was made, owned by, or subject to an obligation of assignment, the same owner, i.e., Legend Design Technology Inc., as evidenced by the Assignment recorded at Reel 010812/Frame 0638.

According to MPEP 706.02(l)(1), because the present application was filed after November 29, 1999, and Applicants have established evidence of common ownership, the Yuan et al. patent is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). Therefore, Applicants respectfully request the rejection be withdrawn.

Conclusion

Based on the reasons as set forth above, Applicants respectfully request allowance of all pending claims.

In the event that there are any questions concerning this paper, or the application in general, the Examiner is respectfully urged to telephone Applicants' undersigned representative so that prosecution of the application may be expedited.

Respectfully submitted,

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